

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Kwan-Yong LIM, et al.

Serial No.: New Application Group Art Unit: Not Yet Assigned

Filed: December 2, 2003 Examiner: Not Yet Assigned

Title: METHOD FOR FABRICATING GATE-ELECTRODE OF SEMICONDUCTOR
DEVICE WITH USE OF HARD MASK

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

December 2, 2003


Sir:

As a means of complying with the duty of disclosure under 37 CFR §1.56, and in accordance with 37 CFR §§1.97 and 1.98, Applicant(s), through the undersigned attorney, submits this Information Disclosure Statement. The patents, publications or other information submitted herewith are listed on the attached Form PTO-1449 and copies are attached.

In accordance with 37 CFR §1.97(b)(1) or (2), this Information Disclosure Statement is being filed either within three months of the filing date of the above-identified application, or within three months of the date of entry into the national stage of the above-identified application as set forth in 37 CFR §1.491. Accordingly, no fee is required.

Respectfully submitted,

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LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.: P69335US0 GROUP ART UNIT: Not Yet Assigned
 SERIAL NO.: New Application FILING DATE: November 2, 2003
 APPLICANT(S): Kwan-Yong LIM, et al. TODAY'S DATE: November 2, 2003

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	INT'L CLASS	SUB- CLASS	FILING DATE (If Appropriate)
_____	AA	<u>6,066,545</u>	<u>05/23/00</u>	<u>Doshi et al.</u>	<u>H01L</u>	<u>21/76</u> <u>12/07/98</u>
_____	AB	<u>6,319,772</u>	<u>11/20/01</u>	<u>Tee et al.</u>	<u>H01L</u>	<u>21/8242</u> <u>10/30/00</u>
_____	AC	<u>6,013,569</u>	<u>01/11/00</u>	<u>Lur et al.</u>	<u>H01L</u>	<u>21/335</u> <u>07/07/97</u>

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION (YES) (NO)
_____	AD	<u>EP 1065715</u>	<u>01/03/01</u>	<u>Europe</u>	<u>H01L</u>	<u>21/8249</u> <u>X</u> _____
_____	AE	_____	_____	_____	_____	_____ _____
_____	AF	_____	_____	_____	_____	_____ _____

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

_____ AG _____

 _____ AH _____

EXAMINER

DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

Information Disclosure Statement

New U.S. Patent Application for
**METHOD FOR FABRICATING GATE-ELECTRODE OF
SEMICONDUCTOR DEVICE WITH USE OF HARD MASK**
Our Ref. No.: P03H5004/US/cj

Reference No.:

- (1) US Patent No. 6,066,545
- (2) US Patent No. 6,319,772
- (3) US Patent No. 6,013,569
- (4) European Publication No. EP 1 065 715 A2